Remarks

Claims 1, 4-5, 7-8, 10, 12-13, 16, and 18-19 are pending in this action. Claims 1, 4-5, 7-8, 10, 12-13, 16, and 18-19 stand rejected. By this amendment claims 1, 10, 13, 16, and 19 have been amended. Applicants respectfully request reconsideration of all pending claims herein. No new matter has been added to the application by virtue of the present amendment.

Claim Objections

Applicants have included the text for the withdrawn claims 21-27 in the present amendment to be in compliance with 37 CFR 1.121(c).

Claim Rejections - 35 U.S.C. § 112 First Paragraph

The Office Action stated that claims 1, 4-5, 7-8, 10, 12-13, 16, and 18-19 stand rejected under 35 U.S.C. §112 first paragraph as failing to comply with the written requirement. Specifically, the Office Action states that independent claims 1, 10, and 16 recite a "black box circuit" or "black box circuit model" but argues that there is no support for either in the specification as filed. Claim 1 is further rejected for claiming a "code module which is created by a program compiler" but that there appears to be no support in the specification for the program compiler; however, clarification is requested if the "program compiler" is an ordinary, well known compiler. The Office Action further stated that claim 1 recites the limitation "wherein the user is prevented from supplying inputs, outputs, and load parameters directly to the simulator module", but that there appears to be no support for this in the application as filed.

Applicants respectfully submit that the language "black box circuit" in the above referenced claims is inherently implied in Applicants' specification (see para 11, 57, 80, and 89),

because "the internals of the specific circuit are hidden from the user" is inherently a black box circuit. The Random House Unabridged Dictionary ©2006 defines black box as "any unit that forms part of an electronic circuit and that has its function, but not its components, specified", The American Heritage® Dictionary of the English Language, Fourth Edition Copyright © 2000 defines black box as "a device or theoretical construct with known or specified performance characteristics but unknown or unspecified constituents and means of operation", and finally, The Free On-line Dictionary of Computing, © 1993-2005 Denis Howe, defines black box as "an abstraction of a device or system in which only its externally visible behavior is considered and not its implementation or 'inner workings'".

In regards to claim 1 claiming "a code module which is created by a program compiler", Applicants have amended claim 1 to recite, "a code module which is formed from a compiled plurality of calls to a simulator module" (see Applicants paragraph 80 and Figure 7) to more precisely claim the invention and thereby overcome the rejection.

In regards to claim 1 claiming "wherein the user is prevented from supplying inputs, outputs, and load parameters directly to the simulator module", Applicants have removed to confusing language to more succinctly claim the invention.

Based on the foregoing clarifications and amendments, Applicants submit that since the 35 U.S.C. §112 first paragraph rejection of claims 1, 10, and 16 has been overcome, the rejection of all other pending claims has also been overcome by virtue of their dependence.

Claim Rejections - 35 U.S.C. § 112 Second Paragraph

The Office Action stated that claims 10-12 are rejected under 35 U.S.C. §112 second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Specifically, the preamble of claim 10 recites "A method of modeling an integrated circuit as a black box circuit so that the integrated circuit details remain hidden **then** (emphasis original) simulating the integrated circuit using the black box circuit model comprising the steps of…" and it appears that the preamble attempts to define method steps, which is unconventional.

Applicants have amended claim 10 to recite a "method of simulating an integrated circuit using a black box circuit model comprising the steps of …" and placed the step of "modeling the integrated circuit as a black box circuit" in the main body of the claim to clarify that final simulation requires a black box circuit model in order to operate. Applicants submit that the rejection to claim 12 has been overcome by virtue of its dependence on claim 10.

The Office Action stated that claim 13 recites "wherein said step of assigning said parameters to said code module comprises the step of providing a call-back function" and that there appears to be a discrepancy between the actor of claim 10, which "assigns inputs…," and the actor of claim 13, which "provides a call-back function," the former apparently a computer user and the latter presumably a component of computer software. The Office Action stated that claim 19 is rejected for the same reasons as the rejection of claim 13. All dependent claims are rejected by virtue of their dependence on their respectively rejected parent claims.

Applicants have amended claims 10, 13, 16 and 19 to clarify that the actor of the respective claims is the interface, which provides the call-back function to the circuit module and specifies to the circuit module which load model has been chosen (see Applicants' paragraph 87

and Fig. 6 element 68). Therefore, Applicants submit that the rejection to claims 13 and 19 for vagueness and indefiniteness has been overcome by virtue of this amendment and thus the rejection of all dependent claims is likewise overcome.

Based on the foregoing clarifications and amendments to claims 10, 13, 16, and 19, Applicants submit that since the 35 U.S.C. §112 second paragraph rejection of claims 10-12, 13, and 19 has been overcome, the rejection of all other pending claims has also been overcome by virtue of their dependence.

Claim Rejections - 35 U.S.C. § 101

The Office Action stated that claims 1, 4-5, 7-8, 10, and 12-13 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The Office Action further stated that claims 1, 4-5, and 7-8 stand rejected because they define a computer software "system" and are therefore nonstatuatory as reciting functional descriptive material *per se*.

The Office Action stated that the method steps described in claims 10, and 12-13 fail to produce a useful, concrete, and tangible result as established in MPEP 2106(II)(A).

The Office Action provided a recitation of 35 U.S.C. § 101 as:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title

Interpretation of 35 U.S.C. §101 is expressed in Diamond, 477 U.S. at 308-309, 206 USPQ at 197, in which the court stated:

> In choosing such expansive terms as "manufacture" and "composition of matter," modified by the comprehensive "any," Congress plainly

> contemplated that the patent laws would be given wide scope. The Committee Reports accompanying the 1952 Act inform us that *Congress intended statutory subject matter to "include anything under the sun that is made by man*."(emphasis added) S. Rep. No. 1979, 82d Cong., 2d Sess., 5 (1952); H.R. Rep. No. 1923, 82d Cong., 2d Sess., 6 (1952). [Footnote omitted]

This perspective has been embraced by the Federal Circuit:

> *The plain and unambiguous meaning of section 101 is that any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may be patented if it meets the requirements for patentability set forth in Title 35* (emphasis added), such as those found in sections 102, 103, and 112. The use of the expansive term "any" in section 101 represents Congress's intent not to place any restrictions on the subject matter for which a patent may be obtained beyond those specifically recited in section 101 and the other parts of Title 35. . . . *Thus, it is improper to read into section 101 limitations as to the subject matter that may be patented where the legislative history does not indicate that Congress clearly intended such limitations* (emphasis added). Alappat, 33 F.3d at 1542, 31 USPQ2d at 1556.

Applicants submit that the claimed invention is statutory because both integrated circuits and the tools that design them are "under the sun" and "made by man". Furthermore, integrated circuits are articles of manufacture, and the simulation system described in Applicants' application and claims 1, 4-5, and 7-8 describes a useful improvement to such circuits. Claims 10 and 12-13 further describe a useful process improvement for integrated circuit design and manufacture.

The statement that claims 10, and 12-13 are rejected under 101 because the elements fail to create a "concrete, and tangible result" would be reading a limitation into section 101 that was not intended by Congress.

MPEP 2106(II)(A) provides guidelines for determining statutory subject matter. Specifically:

> The subject matter sought to be patented must be *a "useful" process*, machine, manufacture, or composition of matter*; i.e., it must have a practical application*.

> The purpose of this requirement is to limit patent protection to inventions that possess a certain level of *"real world" value* (emphasis added), as opposed to subject matter that represents nothing more than an idea or concept, or is simply a starting point for future investigation or research (Brenner v. Manson, 383 U.S. 519, 528-36, 148 USPQ 689, 693-96 (1966); In re Ziegler, 992 F.2d 1197, 1200-03, 26 USPQ2d 1600, 1603-06 (Fed. Cir. 1993)).

Applicants submit that the present invention is a practical, real world application and a useful process for simulating an integrated circuit design to ensure proper functionality *before* costly manufacturing steps are taken. Today few, if any, circuits are manufactured without having first been simulated. Circuit simulation is a critical process step in integrated circuit manufacturing and requires an intricate system to accurately perform the simulation. One step in circuit simulation is the step of modeling a circuit in order to represent it in a data format which can be processed by a computer system (see In re Lowry, 32 F.3d 1579, 1583-84, 32 USPQ2d 1031, 1035 (Fed. Cir. 1994) in which claim to data structure that increases computer efficiency was held statutory.

Furthermore, the invention provides a useful process of circuit simulation. For example, Company A develops a proprietary circuit and sells the circuit to Company B for incorporation into Company B's integrated circuit design. The invention allows Company B to accurately simulate the design without exposing the details of the circuit designed by Company A, thereby maintaining the confidentiality of Company A's circuit design. In another example, Company A may want Company B to manufacture the design, without having access to the circuit details.

Since Applicants' claim 1 is directed to a simulator comprising components that interact to perform the practical function of simulating a proprietary circuit as a "black box circuit", which further has an interface to receive human input, it is statutory subject matter. The practical result of which is simulation data that induces a user to perform a specific task including but not limited to redesign of the circuit or to provide approval to proceed to manufacturing.

In regards to statutory process steps, MPEP 2106 IV(B)(1)(a) states:

> Computer programs are often recited as part of a claim. Office personnel should *determine whether the computer program is being claimed as part of an otherwise statutory manufacture or machine. In such a case, the claim remains statutory irrespective of the fact that a computer program is included in the claim* (emphasis added).

Applicants submit that in the presently claimed invention, a computer program is used in a computerized process where the computer executes the instructions set forth in the computer program to simulate an *integrated circuit* (statutory manufacture) such that the details of the circuit remain hidden to a user. Thus the claimed invention as a whole is a system and process for simulating an integrated circuit using a computer program.

Specifically, independent claim 10 is drawn to "A method of modeling an integrated circuit as a black box circuit so that the integrated circuit details remain hidden comprising the steps of providing a simulator module comprising an API having a plurality of functions; defining a black box circuit by executing said functions; recording a plurality of said functions used by said simulator module during said step of defining said black box circuit to create a plurality of recorded functions; compiling said recorded functions together to create a circuit code module, wherein the code module makes calls to the simulator module during operation; adding an interface to said code module which provides access to said code module from a user program; linking said compiled code module to a circuit simulator; assigning inputs, outputs and load parameters to said code module; and simulating the integrated circuit …", which defines the statutory method steps of performing a circuit simulation which maintains confidentiality of one's circuit design (by modeling the circuit as a black box circuit). The practical result of which is a simulation result that incurs many real world uses including, but not limited to, cost analysis

of manufacturing, redesign of the circuit, or approval to proceed to manufacturing.

MPEP 2106 IV(B)(2)(b)(ii) further specifies statutory criteria for computer-related processes limited to a practical application in the technological arts:

> For such subject matter to be statutory, the claimed process must be limited to a *practical application of* the abstract idea or *mathematical algorithm in the technological arts* (emphasis added). See Alappat, 33 F.3d at 1543, 31 USPQ2d at 1556-57 (quoting Diamond v. Diehr, 450 U.S. at 192, 209 USPQ at 10). See also Alappat at 1569, 31 USPQ2d at 1578-79 (Newman, J., concurring) ("unpatentability of the principle does not defeat patentability of its practical applications") (citing O"Reilly v. Morse, 56 U.S. (15 How.) at 114-19). For example [...] a claimed process for digitally filtering noise employing the mathematical algorithm is statutory.

Applicants' claim 1 is drawn to "A computerized simulation system for simulating an integrated circuit, wherein the simulation system uses a black box circuit model of the integrated circuit such that the integrated circuit details are hidden from a user, comprising...a simulator module... a code module... and an interface through which the user defines said code module...inputs". Therefore claim 1 defines a practical application (circuit simulation for circuit design) in the technological art of integrated circuit electronics.

MPEP 2106 (IV)(B)(2)(b)(i) provides guidance for statutory process claims where physical activities are transformed into computer data:

> Another statutory process is one that requires the measurements of physical objects or activities to be transformed outside of the computer into computer data (In re Gelnovatch, 595 F.2d 32, 41 n.7, 201 USPQ 136, 145 n.7 (CCPA 1979) (data-gathering step did not measure physical phenomenon)), where *the data comprises signals corresponding to physical objects or activities external to the computer system, and where the process causes a physical transformation of the signals which are intangible representations of the physical objects or activities*. Schrader, 22 F.3d at 294, 30 USPQ2d at 1459 citing with approval Arrhythmia, 958 F.2d at 1058-59, 22 USPQ2d at 1037-38; Abele, 684 F.2d at 909, 214 USPQ at 688; In re Taner, 681 F.2d 787, 790, 214 USPQ 678, 681 (CCPA 1982).

Applicants submit that the claimed invention is a statutory process because it requires an

integrated circuit design (physical objects, which may be in the form of a netlist, a layout, GDSII file, etc.) and load parameters (measurements of physical activities) to be input from a user (transformed outside of the computer into computer data) into the computer system. The load data comprises signals corresponding to physical load parameters on the integrated circuit and the simulation process causes a physical transformation of the signals which are intangible representations of the integrated circuit and its operation. The result is a simulated response of how the circuit will perform when it is physically manufactured.

MPEP 2106(II)(C) provides another requirement for determining statutory subject matter. Specifically:

> […] when evaluating the scope of a claim, *every limitation in the claim must be considered*. Office personnel may not dissect a claimed invention into discrete elements and then evaluate the elements in isolation. Instead, *the claim as a whole must be considered.* See, e.g., Diamond v. Diehr, 450 U.S. at 188-89, 209 USPQ at 9 ("In determining the eligibility of respondents' claimed process for patent protection under 101, their claims must be considered as a whole. It is inappropriate to dissect the claims into old and new elements and then to ignore the presence of the old elements in the analysis. *This is particularly true in a process claim because a new combination of steps in a process may be patentable even though all the constituents of the combination were well known and in common use before the combination was made*.").

The claimed process steps of linking, compiling, providing call-back functions, etc. may be old steps known and used in the art, however, the present invention combines these steps along with a new step of modeling a black box circuit such that the details of the circuit remain hidden from the user, which further comprises steps that include recording function calls, compiling the recorded function calls, providing call-back functions, integrating at least one API, creating code and simulation modules, and providing a user interface that successfully provides user inputs to the model.

The Office Action further stated that the recited steps in claims 10 and 12-13 fail to achieve either "simulating" or "modeling" and that these acts also fail to produce a useful, concrete, and tangible result in isolation (see Office Action pg. 6 item 5).

Applicants respectfully disagree that the present invention fails to achieve either "simulating" or "modeling" and request clarification as to why Examiner believes the steps fail to achieve "simulating" or "modeling", when, in fact, claim 10 recites "A method of *modeling an integrated circuit as a black box circuit* so that the integrated circuit details remain hidden comprising…*defining a black box circuit*…recording a plurality of … functions used by said simulator module during said step of defining said black box circuit … compiling said … functions together to create a circuit code module… and *simulating the integrated circuit* …" and achieves both "simulating" and "modeling" (an integrated circuit).

Based on the foregoing, Applicants submit the invention is statutory because a system (i.e. the simulation system) and process for simulating a circuit design are both useful and have a practical application to the technological art of the design of integrated circuits. Therefore, Applicants submit that claims 1 and 10 as amended are statutory under the definition of 35 U.S.C. §101 and respectfully submit that the rejection of claims 1 and 10 has been overcome. Likewise, the rejection of claims 4-5, 7-8, and 12-13 is also overcome by virtue of their dependence.

Claim Rejections - 35 U.S.C. § 102(b)

The Office Action stated that claims 1, 5, 7, 10, 12-13, 16, and 18-19 are rejected under 35 U.S.C. §102(b) as being anticipated by US Patent No. 6,077,304 issued to Kasuya. The Office Action stated that claim 1 is rejected because Kasuya teaches a circuit simulator engine comprising an API

Applicants respectfully submit that Kasuya does not teach the element of Applicants claim 1 regarding the components (specifically the code module) and steps necessary to simulate

the circuit behavior of a black box circuit (specifically recording function calls and compiling the recoded functions into a code module). Kasuya does not teach "…a simulator module comprising an API wherein said API comprises at least one function; wherein said *simulator module uses said function to define a component of the black box circuit and its corresponding simulated behavior*; and wherein *said function is recorded as a recorded function* and *said recorded function, when called during a simulation, reproduces a behavior corresponding to the black box circuit;* a *code module which is formed from a compiled plurality of recorded functions* wherein the code module makes calls to the simulator module during simulation of the black box circuit…" Rather, Kasuya teaches a simulation engine that simulates the operation of the circuit specified by the *HDL circuit specification* and not a black box circuit, which is specified by plurality of recorded functions which have been compiled into a code module (see Kasuya Col.4 lines 25-28). The HDL circuit specification defined in Kasuya is not a black box circuit specification. It is a specification including all details of every circuit in the design.

Furthermore, Kasuya simulates the operation of circuit components in accordance with predefined circuit models, which are typically stored in a library (see Kasuya Col.4 lines 32-35). Applicants' black box circuit is a plurality of recorded function calls that have been compiled into a functional code module (not a predefined static circuit model). The code module makes calls to the simulator module when black box circuit model behavior information is needed during simulation (See Applicants' abstract, summary, paragraphs 8-11, 89, 102, Fig. 7, and claims 1, 7, 10 and 16).

Therefore, Applicants submit that the 35 U.S.C. §102 rejection of claim 1 as being anticipated by Kasuya has been overcome because Kasuya fails to anticipate all of the elements of claim 1, therefore, the rejection of claims 5 and 7 is overcome by virtue of their dependence on

claim 1. Independent claims 10 and 16 as amended are not anticipated by Kasuya for the reasons stated above regarding claim 1. Therefore, the rejection of claims 12-13 is also overcome by virtue of their dependence on claim 10 and the rejection of claims 18-19 is overcome by virtue of their dependence on claim 16. Applicants therefore submit that the 35 U.S.C. § 102 rejection of claims 1, 5, 7, 10, 12-13, 16, and 18-19 has been overcome and all claims are in condition for allowance.

Claim Rejections - 35 U.S.C. § 103(a)

The Office Action stated that the Application currently names joint inventors (Office Action pg. 12-13). Applicants are unaware of any claims that were not commonly owned at the time of the invention. Applicants request a call from the Examiner if there are further questions in this regard.

The Office Action stated that claims 4 and 8 are rejected under 35 U.S.C. § 103(a), as being unpatentable over U.S. Patent No. 6,077,304 issued to Kasuya (Kasuya) in view of "How Computers Work, 6th Edition" by Ron White (White), further in view of "IEEE 100 The Authoritative Dictionary of IEEE Standards Terms, Seventh Edition" (IEEE), further in view of "Microsoft Computer Dictionary, Fifth edition" (Microsoft). The Office Aciton stated that Kasuya discloses a circuit simulator implemented on a computer system including a user interface and an API to control the simulator. The Examiner further stated that White and Microsoft disclose concepts such as dynamic link libraries and that IEEE discloses definitions for APIs.

In establishing a case of prima facie obviousness, the court stated in *Ortho-McNeil Pharm., Inc. v. Mylan Labs, Inc., 2006 U.S. Dist. LEXIS 34476*, that:

> In determining obviousness, the PTO employs a two-step analysis. First, it considers whether or not the prior art demonstrates a "prima facie" case of obviousness. The prima facie case is a procedural tool that requires that the examiner initially produce evidence sufficient to support a ruling of obviousness. *In re Kumar, 418 F.3d 1361, 1366 (Fed. Cir: 2005*) (citations omitted). To establish a prima facie case of obviousness, there must be (1) some suggestion or motivation in the prior art references or "in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine" its teachings; (2) a reasonable expectation of success in doing so; and (3) the prior art references "must teach or suggest all the claim limitations" of the claimed invention. Manual of Patent Examining Procedures ("MPEP") § 706.02(j) (2005). "The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure."

Therefore, in order to create a prima facie case of obviousness under 35 U.S.C. §103 the references must teach or suggest all limitations of the claimed invention (see MPEP § 706.02(j) (2005)). Since Kasuya does not anticipate all of the elements of claim 1 from which claims 4 and 8 depend (specifically for lack of teaching in regards to a code module made from compiled recorded functions which provides black box circuit model behavior information during simulation) and because none of the references IEEE, Microsoft or White teach or suggest all of the elements or limitations of claims 4 or 8 in combination with Kasuya, the obviousness rejection of claims 4 and 8 has been overcome.

It is also a requirement that the PTO avoid using hindsight during examination. In other words, the applicant's invention cannot be used as a blueprint to search for prior art, which, when combined, results in applicant's invention.

In re Rouffet, 149 F.3d 1350, 1358 (Fed. Cir. 1998), the court stated:

> To prevent the use of hindsight based on the invention to defeat patentability of the invention, the courts require the examiner to show a motivation to combine the references that create the case of obviousness. In other words, the examiner must show reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed. [...] This court forbids

> the use of hindsight in the selection of references that comprise the case of obviousness. See *In re Gorman, 933 F.2d 982, 986, 18 U.S.P.Q.2D (BNA) 1885, 1888 (Fed. Cir. 1991)* [...] When it is necessary to select elements of various teachings in order to form claimed invention, a court ascertains whether there is any suggestion or motivation in prior art to make selection made by applicant. Obviousness can not be established by combining teachings of prior art to produce the claimed invention, absent some teaching, suggestion, or incentive supporting the combination. [...] It is impermissible, however, simply to engage in hindsight reconstruction of claimed invention, using applicant's structure as template and selecting elements from references to fill gaps. References themselves must provide some teaching whereby applicant's combination would have been obvious. See *In re Gorman, 933 F.2d 982 (Fed. Cir. 1991).*

Further, the CAFC, in *In Re Oetiker, 24 USPQ 2.d 1443, 1445 (CAFC 1992)* held:

> There must be some reason, suggestion, or motivation found in the prior art whereby a person of ordinary skill in the field of the invention would make the combination. That knowledge can not come from the applicant's invention itself.

In the case of In Re Dembiczak, 50 USPQ 2.d 1614 (CAFC 1999) the CAFC held:

> Our case law makes clear that the best defense against the subtle but powerful attraction of a hindsight-based obviousness analysis is rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references. See, e.g., *C.R. Bard, Inc. v. M3 Sys., Inc., 157 F.3d 1340, 1352, 48 U.S.P.Q.2D (BNA) 1225, 1232 (Fed. Cir. 1998)* (describing "teaching or suggestion or motivation [to combine]" as an "essential evidentiary component of an obviousness holding"); *In re Rouffet, 149 F.3d 1350, 1359, 47 U.S.P.Q.2D (BNA) 1453, 1459 (Fed. Cir. 1998)* ("the Board must identify specifically . . . the reasons one of ordinary skill in the art would have been motivated to select the references and combine them"); *In re Fritch, 972 F.2d 1260, 1265, 23 U.S.P.Q.2D (BNA) 1780, 1783 (Fed. Cir. 1992)* (examiner can satisfy burden of obviousness in light of combination "only by showing some objective teaching [leading to the combination]"); *In re Fine, 837 F.2d 1071, 1075, 5 U.S.P.Q.2D (BNA) 1596, 1600 (Fed. Cir. 1988)* (evidence of teaching or suggestion "essential" to avoid hindsight); *Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 297, 227 U.S.P.Q. (BNA) 657, 667 (Fed. Cir. 1985).*

Since there is no teaching, motivation or suggestion in any of the cited references to combine the teachings of Kasuya with the IEEE, Microsoft and White references, one of ordinary skill in the art would not have been motivated to create a code module from compiled recorded function calls, such that the code module has the ability to simulate a black box circuit whose circuit details are hidden from the user. Furthermore, the White, IEEE, and Microsoft references show only fundamental electronic principles and rudimentary software programming techniques and would not have provided one of ordinary skill in the art at the time of the invention with the enablement to make and practice the invention.

Applicants have amended claim 1 to clarify the claimed invention, as noted above, and thus patentably distinguish it from the references cited by the Examiner. Accordingly, Applicants respectfully submit that the rejection of claims 4 and 8 under 35 U.S.C. § 103(a) has been overcome and all claims are in condition for allowance.

Summary and Conclusion

Based on the foregoing, it is respectfully submitted that the pending claims in the subject patent application are in condition for allowance and that the application may be passed to issuance.

The Examiner is urged to call the undersigned at the number listed below if, in the Examiner's opinion, such a phone conference would aid in furthering the prosecution of this application.

Respectfully submitted,
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